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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,437	11/24/2003	Walter Anthony Wohlmuth	TRQ-00004	7134

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EXAMINER	
NGUYEN, DAO H	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,437	WOHLMUTH, WALTER ANTHONY	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *18/27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1103 & 0404 & 0305*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 11/24/2003 through 08/29/2005.

Claims 1-27 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 08/29/2005. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Applicant made a provisional election without traverse to prosecute the invention of Group I, claims 1-17, drawn to semiconductor devices. Affirmation of this election was made in the Response to Restriction Requirement filed 08/29/2005.

Claims 18-27 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group there being no allowable generic or linking claim.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Drawings

3. The drawings are objected to for the following reasons.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "solid state amorphization region" beneath the D-mode gate contact within the first layer as described in claims 7 and 14, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

The drawings are objected to under 37 CFR 1.83(a) because they fail to show the substrate "10" as described in the specification, page 3, line 16. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected to for the following reason:

In the specification , page 4, lines 9 and 12, the reference numbers "90" for the ohmic contact layer should be changed to –28-- as defined on line 1 of the same page. Similarly, the reference number "28" for the E-mode barrier layer on page 5, line 6 should be changed to –18--; the E-mode etch stop layer reference number "50" on page 8, line 2 should be changed to 20. Otherwise, appropriate correction(s) must be made.

In addition, the lengthy specification has not been checked to the extent necessary to determine the presence of any possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim(s) 1 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by admitted prior art (Admission).

Regarding claim 1, Admission discloses an integrated circuit, as shown in fig. 1 of the instant application, comprising:

a depletion mode (D-mode) field effect transistor (FET) 2 and an enhancement mode (E-mode) FET 3 in a multi-layer structure 5, wherein the multi-layer structure 5 includes a semiconductor substrate 12 overlaid with a plurality of epitaxial semiconductor common to the D-mode and E-mode FETs 2/3, including a channel layer 16 overlaid by barrier layers 18/22 overlaid by a first layer 28, wherein the D-mode and E-mode FETs 3/4 each include a source contact 38, a drain contact 40, and a gate contact 30/34, and wherein the respective source and drain contacts 38/40 of the D-mode FET and E-mode FET are coupled to the first layer 28, and the respective gate contacts 30/34 of the D-mode FET and E-mode FET are coupled to the barrier layer 22/18.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim(s) 2-17 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over admitted prior art (Admission) in view of U.S. Patent No. 6,452,221 to Lai et al.

Regarding claim 2, Admission discloses the integrated circuit comprising all claimed limitations, except for a solid state amorphization region beneath the E-mode gate contact at least within the barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the E-mode gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Admission to have a solid state amorphization region be beneath the E-mode gate contact as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 3, Admission/Lai discloses the integrated circuit wherein the solid state amorphization region includes at least one compound including at least one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 4, Admission/Lai discloses the integrated circuit wherein the solid state amorphization region includes a plurality of compounds, wherein at least one of the compounds includes one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium, and at least one of the compounds includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 5, Admission/Lai discloses the integrated circuit wherein the multi-layer structure further comprises at least an epitaxial second layer 26 between the barrier layer 20 and the first layer 28. See admitted fig. 1.

Regarding claim 6, Admission/Lai discloses the integrated circuit wherein the barrier layer is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the solid state amorphization region is within the implant region. See admitted fig. 1; and fig. 1 and col. 2, lines 55-65 of Lai.

Regarding claim 7, Admission discloses an integrated circuit, as shown in fig. 1 of the instant application, comprising:

a depletion mode (D-mode) field effect transistor (FET) 2 and an enhancement mode (E-mode) FET 3 in a multi-layer structure 5, wherein the multi-layer structure 5 includes a semiconductor substrate 12 overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETs 2/3, including a channel layer 16 overlaid by a barrier layer 18 overlaid by a first layer 22 overlaid by a second layer 28, wherein the D-mode and E-mode FETs 2/3 each include a source contact 38, a drain contact 40, and a gate contact 30/34, and

wherein the source and drain contacts 38/40 of the D-mode FET and the E-mode FET 2/3 are coupled to the second layer 28, wherein the gate contact 30 of the D-mode FET 2 is coupled to the first layer 22, and

wherein the gate contact 34 of the E-mode FET 3 is coupled to the barrier layer 18.

Admission does not teach about a solid state amorphization region beneath the D-mode gate contact within the first layer and a solid state amorphization region beneath the E-mode gate contact within the barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Admission to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 8, Admission/Lai disclose the integrated circuit wherein the multi-layer substrate includes an epitaxial third layer 20 between the first layer 22 and the barrier layer 18, said third layer 20 having a different composition than the first layer 22 and the barrier layer 18, and wherein the D-mode solid state amorphization region is within the third layer. See admitted fig. 1, and fig. 1 of Lai.

Regarding claim 9, Admision/Lai discloses the integrated circuit wherein the barrier layer is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the E-mode solid state amorphization region is within the implant region. See admitted fig. 1; and fig. 1 and col. 2, lines 55-65 of Lai.

Regarding claim 10, Admision/Lai discloses the integrated circuit wherein the D-mode and E-mode solid state amorphization regions include at least one compound

including platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 11, Admission/Lai disclose the integrated circuit wherein the at least one of the D-mode and E-mode solid state amorphization regions includes a plurality of compounds, wherein at least one of the compounds includes one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium,
and at least one of the compounds includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 12, Admission discloses an integrated circuit, as shown in fig. of the instant application, comprising:

a depletion mode (D-mode) field effect transistor (FET) 2 and an enhancement mode (E-mode) FET 3 in a multi-layer structure 5, wherein the multi-layer structure 5 includes a semiconductor substrate 12 overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETS, including a channel layer 16 overlaid by a barrier layer 18 overlaid at least by a first layer 22; wherein the D-mode and E-mode FETs each include a source contact 38, a drain contact 40, and a gate contact 30/34, and wherein the source and drain contacts of the D-mode FET and the E-mode FET are coupled to one of the epitaxial layers 28 overlying the channel

layer 16, wherein a gate contact 30 of the D-mode FET 2 is coupled to one of the first and barrier layers 22, and wherein a gate contact 34 of the E-mode FET 3 is coupled to one of the first and the barrier layers 18.

Admission does not teach about a solid state amorphization region being present beneath the E-mode gate contact at least within the barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the E-mode gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Admission to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 13, Admission/Lai discloses the integrated circuit wherein the D-mode gate contact 30 is coupled to the first layer 22, and the E-mode gate contact 34 is coupled to the barrier layer 18. See admitted fig. 1.

Regarding claim 14, Admission/Lai discloses the integrated circuit further comprising a second solid state amorphization region disposed beneath the D-mode gate contact at least within the first layer. See the rejection of claim 7.

Regarding claim 15, Admission/Lai discloses the integrated circuit wherein the D-mode and E-mode source and drain contacts are coupled to the first layer, and the D-mode and E-mode gate contacts are coupled to the barrier layer. See admitted fig. 1.

Regarding claim 16, Admission/Lai discloses the integrated circuit wherein the D-mode and E-mode source and drain contacts are coupled to the first layer, and the E-mode gate contact is coupled to the barrier layer. See admitted fig. 1.

Regarding claim 17, Admission/Lai discloses the integrated circuit wherein the barrier layer is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the E-mode solid state amorphization region is within the implant region. See admitted fig. 1; and fig. 1 and col. 2, lines 55-65 of Lai.

Conclusion

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
September 16, 2005